EECS 151/251 A
Discussion 2

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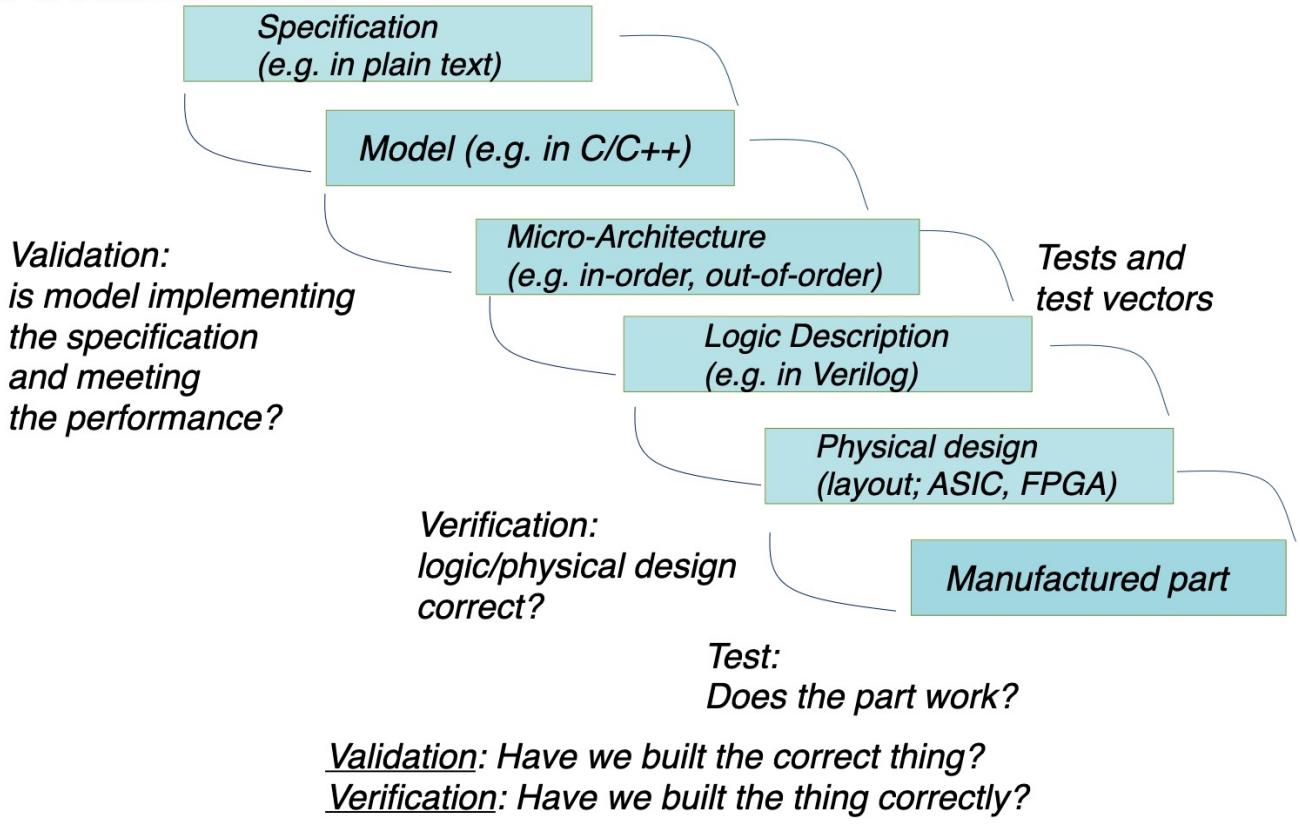
Clarification: Power Dissipated vs Power Density

- Power dissipated = Power Emitted as heat from the resistance of the circuit. This power scales with $(1/k^2)$ as the chip scales since the current and the voltage scale by $1/k$
- Power density = Power used by the circuit (to switch on/off the transistors) per unit area. This power stays constant with Dennard Scaling
- So is the power dissipated also per unit area? Well, it does not matter: the voltage and current are both independent of the area. If you have more area, you will still dissipate the same amount of power

Overcoming Digital Design Challenges

- Hierarchy
- Use CAD tools



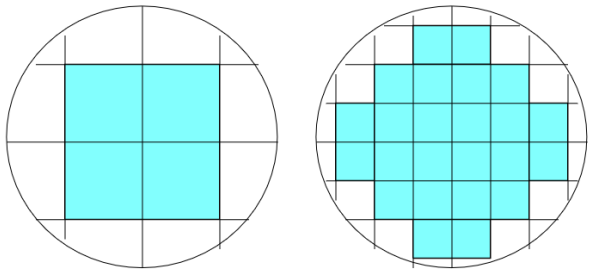
Design Tradeoffs

- NRE Costs (Non-Recurring Engineering) Costs
  - Employees, tools, masks
- Recurring Costs
  - Manufacture, test, and package
- Performance: Throughput, Latency
- Energy and Power

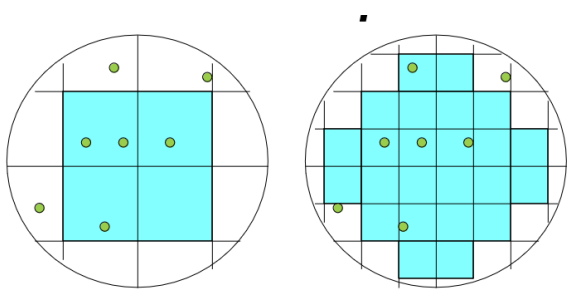
Die Cost

- Dies are built onto a larger chip: Wafer
- Yield : Percent of dies that work
- Cost per die = Cost per wafer / dies per wafer * die yield
- Wafer is a circle, while dies are square
- alpha is approx. 3

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Yield = 0.25



Yield = 0.76

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

Circuit Implementation

- Standard cell ASICs (most common)
  - Use EDA tools to go from Verilog -> layout
    - does PnR automatically for defined gates
- Full-custom ASICs
  - Manually layout every transistor (can design macro blocks this way)
  - Can hyper optimize die area efficiency/etc.

Design Tradeoffs

- ASICs
  - Expensive to develop, cheap per die cost
  - Long Verification
- FPGAs
  - More expensive parts, much easier to develop
  - More configurable than ASICs
  - Lower performance and energy efficiency than an ASIC
- Processors (SW)
  - Easy to design (sequential execution, just write code)
  - Even lower performance and Energy-efficiency

Problem 1

Problem 3: Die Cost

You are fabricating $150\,\text{mm}^2$ dies on $300\,\text{mm}$ wafers with $\alpha = 3$ and a defect per unit area $0.005\,/\text{mm}^2$. Each wafer costs \$20k. How much does each die cost?

Solution

Solution:

$$\text{Die Yield} = \left(1 + \frac{0.005\,/\text{mm}^2 \cdot 150\,\text{mm}^2}{3}\right)^{-3} = 0.512$$

$$\text{Dies per wafer} = \frac{\pi \cdot (300\,\text{mm}/2)^2}{150\,\text{mm}^2} - \frac{\pi \cdot 300\,\text{mm}}{\sqrt{2 \cdot 150\,\text{mm}^2}} \approx 417$$

$$\text{Die Cost} = \frac{\$20,000}{417 \cdot 0.512} \approx \$94$$

Problem 2

Imagine you are designing a product with embedded processing. Your job is to choose the appropriate implementation approach for the processing part of your product. You are given the following choices. Rank order the following design alternatives by filling in the table with 1,2,3,4 representing the relative ranking (1 being the lowest and 4 being the highest). Rank based on the best-case design in each category. If there is a tie, use the lower number (e.g. if tied for 2 or 3, use 2). Flexibility means flexibility after fabrication. Per-die cost of Processor is not required.

	Full-Custom	Std Cell ASIC	FPGA	Processor
NRE Cost				
Performance				
Energy Efficiency				
Per Die Cost				-
Flexibility				

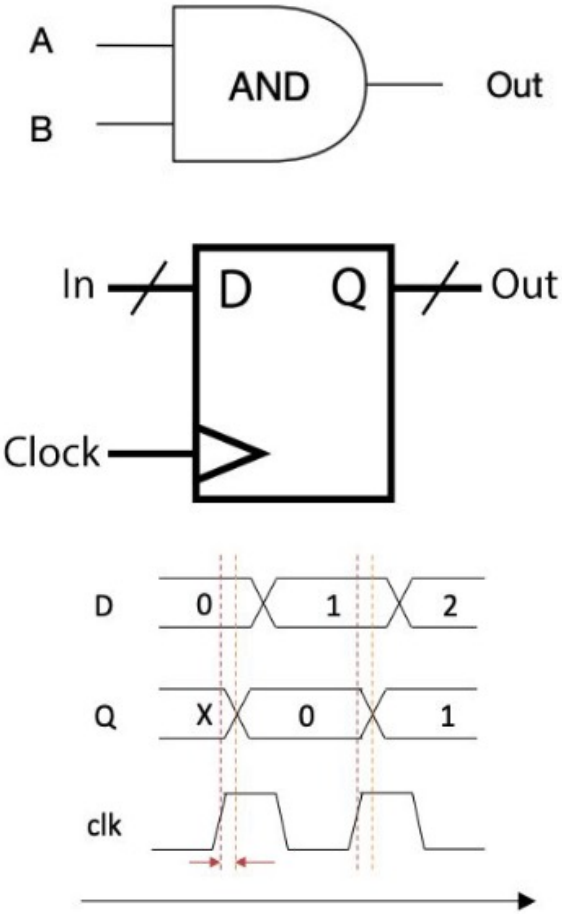
Solution

Solution:

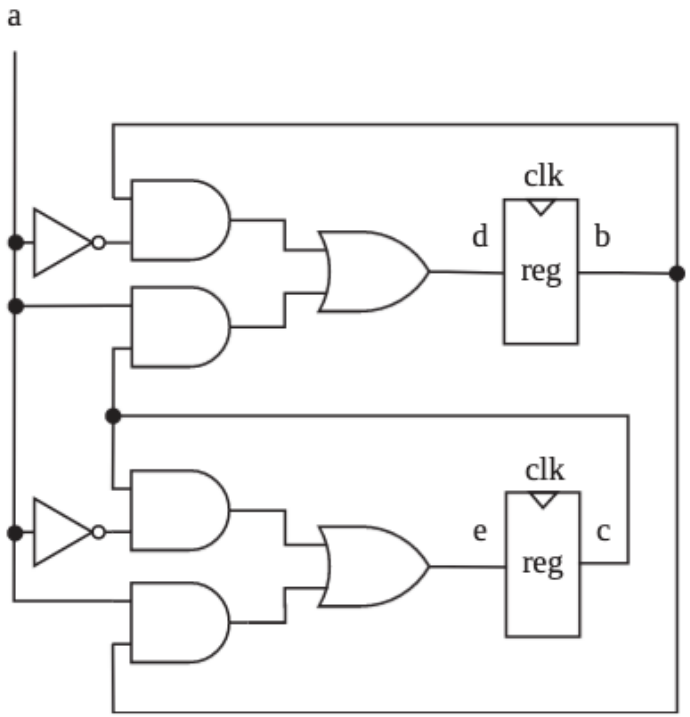
	Full-Custom	Std Cell ASIC	FPGA	Processor
NRE Cost	4	3	2	1
Performance	4	3	2	1
Energy Efficiency	4	3	2	1
Per Die Cost	1	2	3	-
Flexibility	1	1	2	2 (or 3)

Logic Circuits

- Combinational and Sequential Elements
- Combinational elements have their outputs change (almost) immediately
- Sequential elements change output on the inputted clock signal.
  - Example is Flip Flops, latches, Registers, etc.



For the sequential logic circuit with input a and output f shown below,



(a) Show the truth table of the combinational part (use a, b, and c as input, and d and e as output).

(b) Complete the following table.

cycle	0	1	2	3	4
a	0	1	1	0	1
b	1	1	0		
c	0	0	1		
d	1	0			
e	0	1			

Solution

(a)

a	b	c	d	e
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

(b)

cycle	0	1	2	3	4
a	0	1	1	0	1
b	1	1	0	1	1
c	0	0	1	0	0
d	1	0	1	1	0
e	0	1	0	0	1