

EECS 151/251 A

Discussion 6

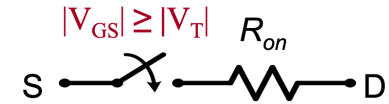
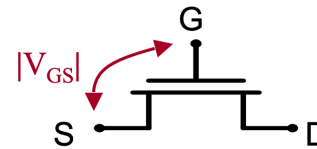
Feb 23, 2024

Content

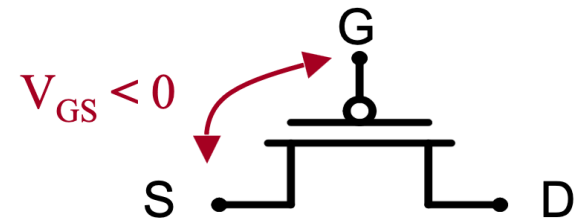
- Transistors
- Pull up/ Pull down
- Circuit Layouts
- Problems

Transistors

MOS Transistor ↔ A Switch!

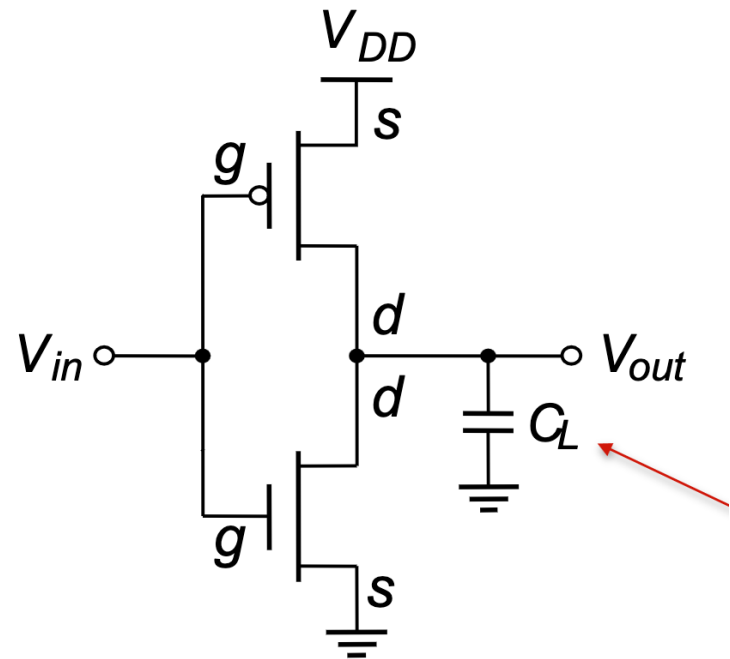


- NMOS and PMOS
- Bidirectional, but usually configured to work one way
- We abstract as a switch with resistance! There is actually some leakage current (I_{off}) even when $V_{GS} < V_T$
- What does raising/lowering V_T do to I_{off} and I_{on} ?
- Resistance of transistor is not actually linear! But we approximate in this class



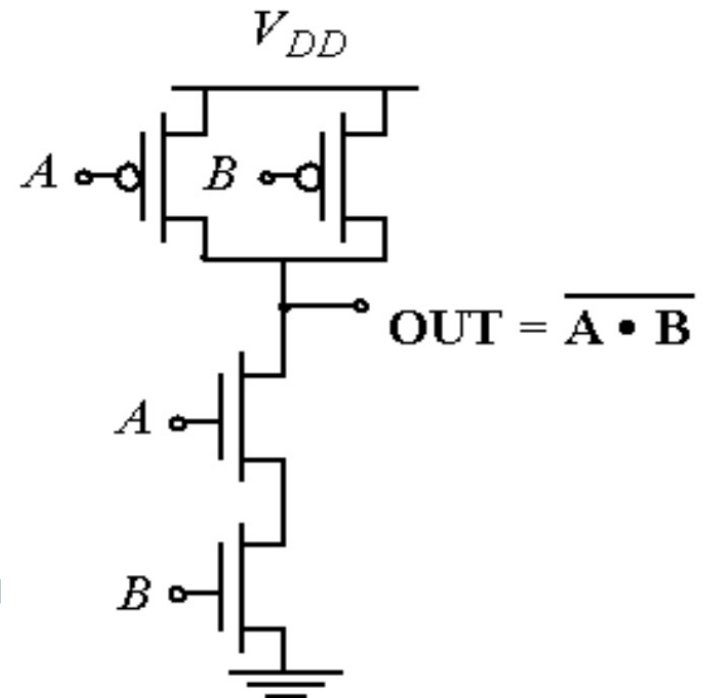
Connecting Transistors

- C_L models the capacitance of the entire system
- What gate is this showing?
- Note that V_{out} is either directly connected to ground or V_{DD} , except for brief periods when switching
- Why does PMOS connect V_{DD} while NMOS connects ground?



Pull-Up vs Pull-Down

- Pull-Up: PMOS transistors that connect V_{DD} to V_{out}
- Pull-Down: NMOS transistors that connect ground to V_{out}
- AND: Transistors in series
- OR: Transistors in parallel
- Pull-Up complements Pull-Down

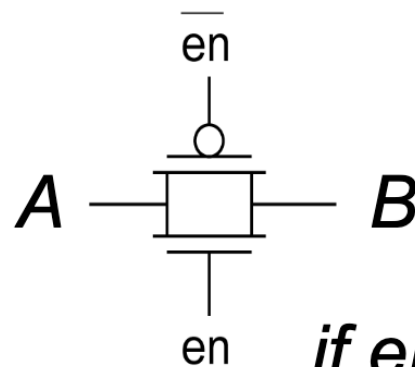


Pull-Up vs Pull-Down

- Pull-Up generates all 1s in truth table, Pull-Down generates all 0s
- Can you generate an AND gate (as a single gate)?
- Series connections in Pull-down are parallel in Pull-Up and vice versa (DeMorgan's)
- This ensures that pull-down and pull-up are never triggered at once!

Static Gates vs Transmission Gates

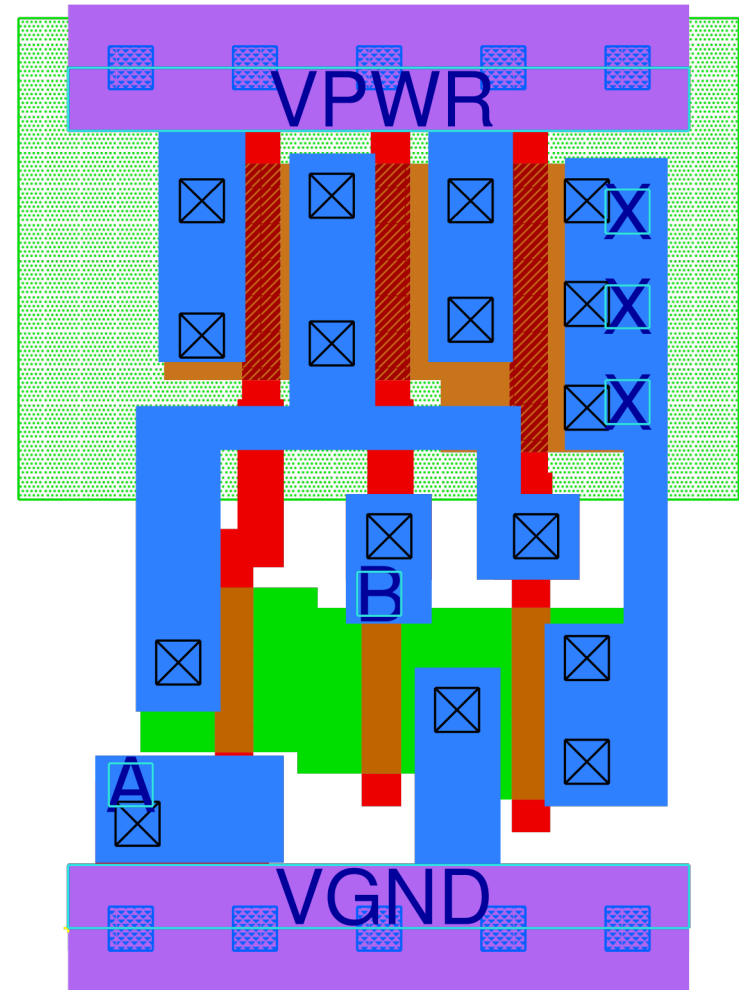
- Static Gates connect to V_{DD} and ground
- Transmission gates connect A to B via idealized “switch”
- Can't connect too many transmission gates in a row. Why?



if $en == 1$ then A connects to B

Circuit Layouts

- What is this?

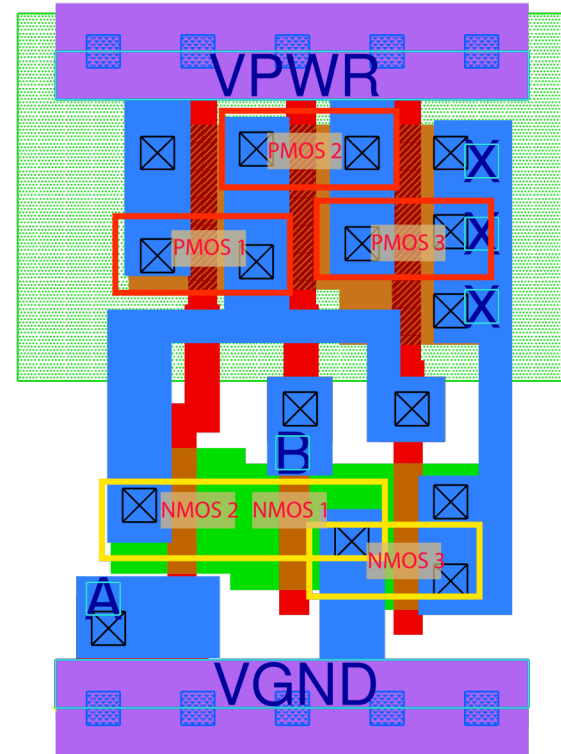
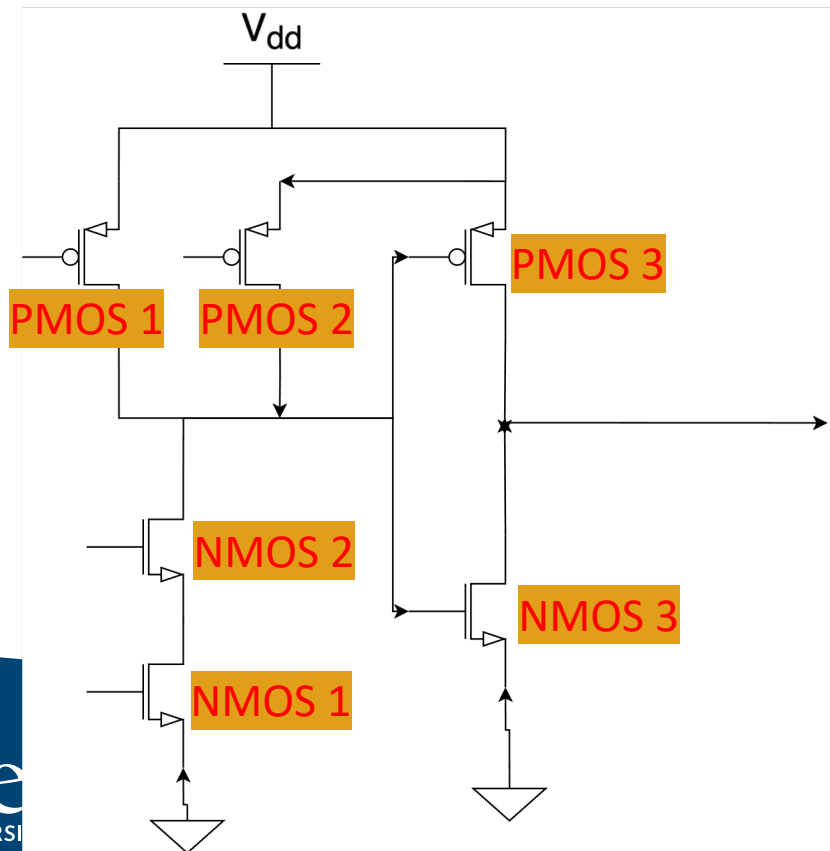


Circuit Layouts

- AND Gate!

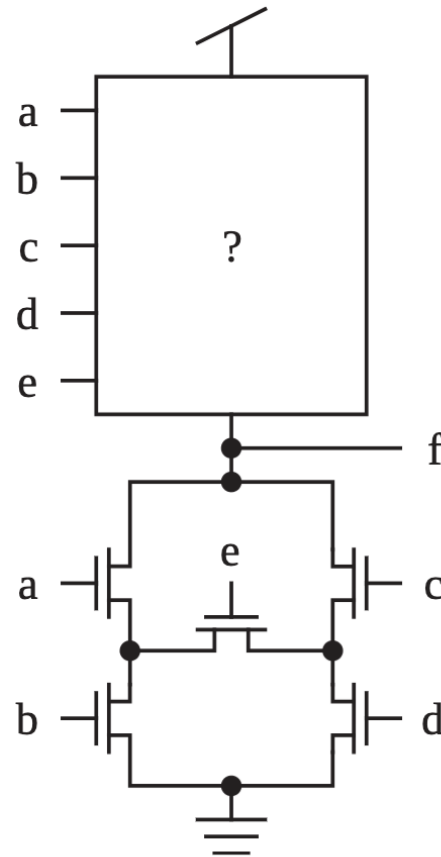
Circuit Layouts

- What is this?



Problem 1

Complete the following CMOS schematic with inputs a, b, c, d, e and output f . Also, write a Boolean expression of the output f .

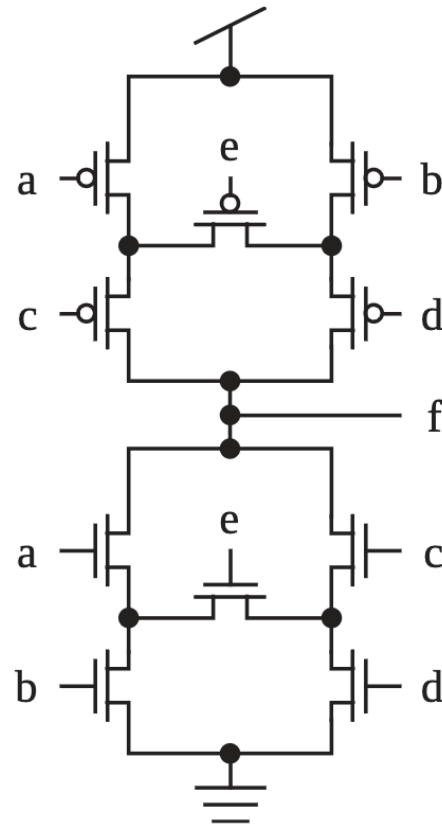


Solution

Solution:

Function:

$$f = (ab + cd + aed + bce)' \quad (1)$$



Problem 2

Write a CMOS schematic for $f = a'b' + b'c' + c'a'$.

Solution

Function:

$$f' = (a + b)(b + c)(c + a) = ab + bc + ca = a(b + c) + bc \quad (2)$$

Schematic:

