EECS 151/251 A Discussion 7

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Content

- Performance
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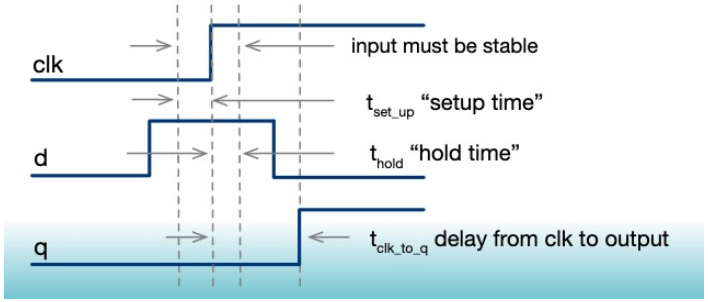
- Gate Delay
- Wire Delay
- Retiming

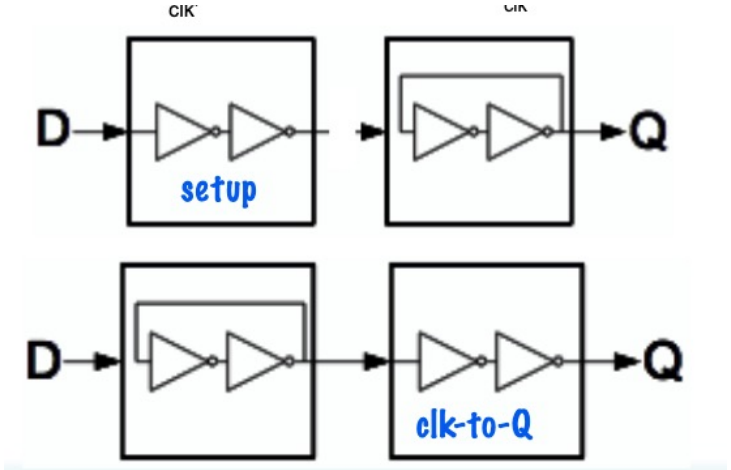
Performance

- Performance is proportional to clock frequency
- Need to minimize the critical delay in each clock cycle
  - Logic Gate Delay
  - FF Delay
  - Interconnect Delay
- **All signals must be ready (“setup”) before clock rising edge!**

FF Timing Requirements

- 3 important times for FFs:
  - Setup: How long D should be ready before clock edge
  - Hold: How long D should last after clock edge
  - Clock to Q: How long it takes Q to become D after edge
- "Slack"
  - Setup Slack: Setup Required Time (based on set up time) – Arrival Time Hold Slack: Arrival Time – Hold Required Time
  - Positive Slack is good/no violations
  - How do you calculate Arrival Time, Setup Required Time, Hold Required Time?

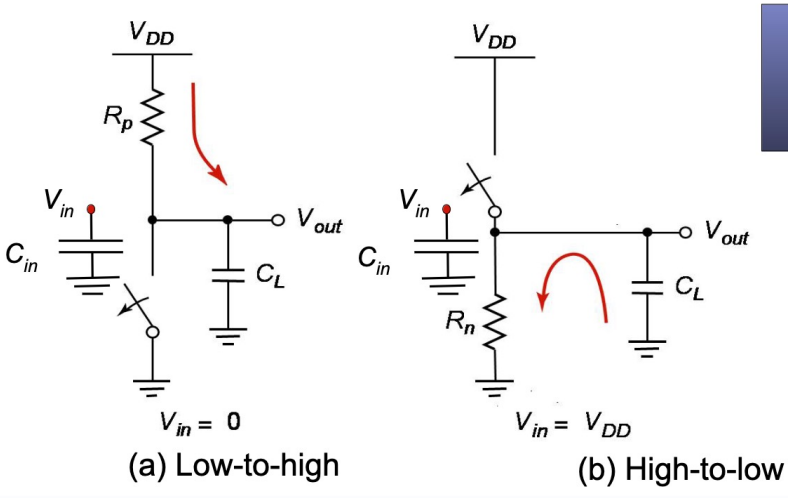




Gate Delay

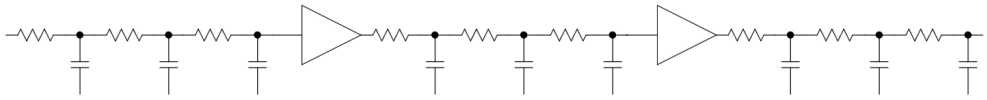
- Transistors are not perfect switches
- Use C_L to model capacitance of entire load (output, wires, etc.)
- Transistor strength is proportional to W/L
- Time it takes for voltage to change is gate delay

$$t_{pHL} = f(R_{on}C_L) = 0.69\,R_n\,C_L$$



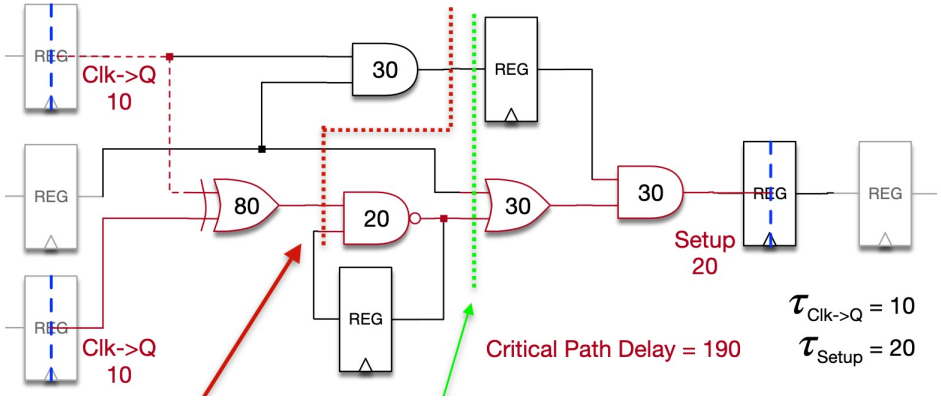
Wire Delay

- On top of FF delay and Logic Gate Delay, there is additional delay from the interconnects
- Delay caused by resistance and capacitance
  - Both are determined by length of wire
- Short Wires
  - R is relatively insignificant, so C is important for gate load (which we will delve more into next week)
- Long wires
  - Distributed RC effect
  - Time constant is proportional to square of the length of the wire
  - May require rebuffering



Retiming

- Move logic between different registers to balance delay
- Time taken between registers should be equalized
  - Clock frequency has to work for slowest section. This is the critical path
- Remember that adding a register adds a setup time and c2q time (as well as more space on the chip)!



Retiming steps

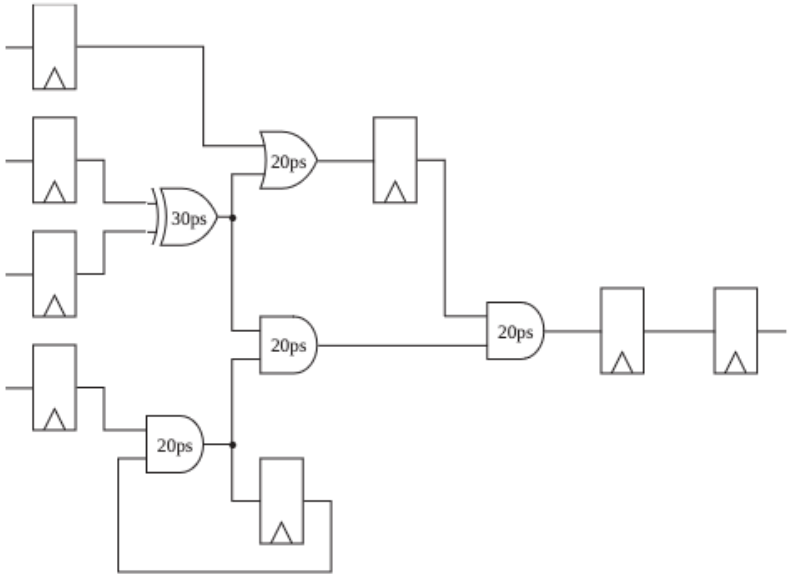
Loop:

1. Calculate Critical Path
2. Look for a spot along the critical path you can add a register
3. In more complicated examples, may be able to combine registers if you know their initial values

Problem 1

Problem 1: Retiming

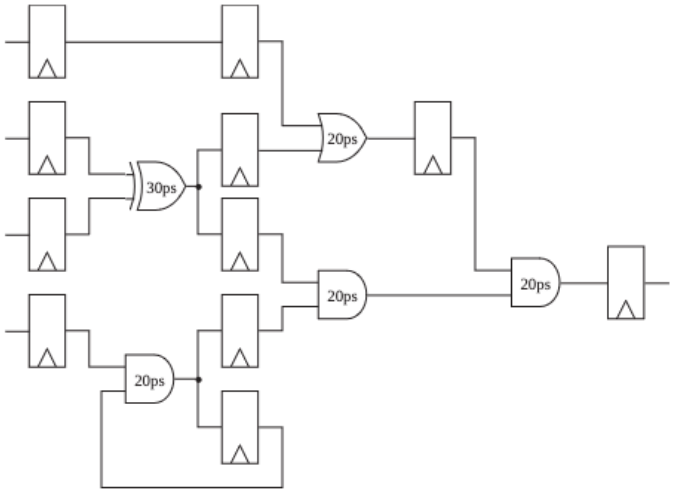
Consider the circuit below. What is the maximum clock frequency? Retime the circuit to minimize the critical path delay. What is the maximum clock frequency for the retimed circuit? Also show the diagram of the retimed circuit. The FFs have $t_{setup} = 10\text{ps}$, $t_{clk-q} = 10\text{ps}$, and $t_{hold} = 5\text{ps}$.



Solution

Solution:

Original maximum clock frequency: $\frac{1}{10+10+30+20+20\text{ps}} \approx 11.1\text{GHz}$.
(The hold time constraint does not matter because clock to q delay is larger.)
Retimed maximum clock frequency: $\frac{1}{10+10+20+20\text{ps}} \approx 16.6\text{GHz}$.
Diagram:



Note: The following diagram is wrong because it merges two FFs at the fanout of XOR gate even though we are not given initial values of FFs.