# EECS 151/251 A Discussion 9

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# Content

- Timing Requirements
- Single Cycle RISC-V

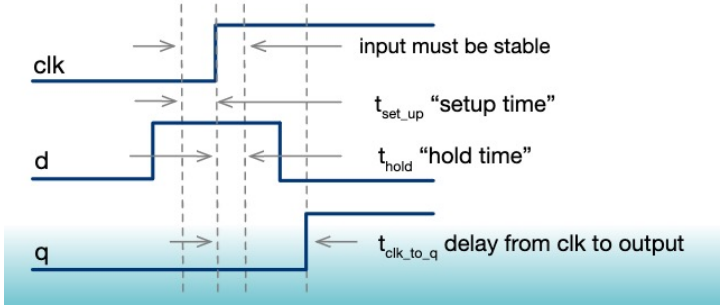
# Timing Recap

- Arrival Time – Time that the input to the FF arrives
- Setup Time – Time which input must be stable ***before*** the positive edge of clock
- Hold Time – Time data at input must be stable ***after*** the positive edge of clock

$$Arrival\ Time = T_{clk \to q} + T_{comb}$$

$$Setup\ Time: T_{clk} - T_{clk \to q} - T_{setup} \geq T_{comb} - T_{skew} *$$

$$Hold\ Time: T_{clk \to q} + T_{comb} \geq T_{hold} + T_{skew} *$$




*Skew will be covered in future lectures. Generally positive skew is good for setup, and bad for hold

# Retiming Correction

Kevin incorrectly said retiming is similar to pipelining. He was wrong!

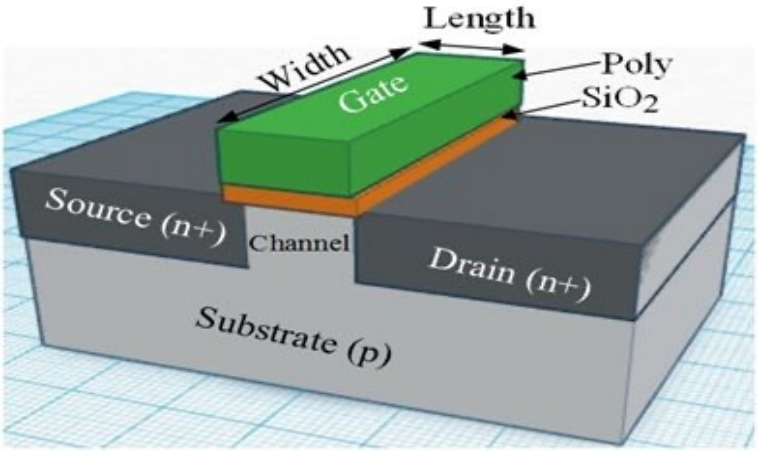
Retiming is about balancing the existing delays in the circuit in order to reduce the critical path, but the cycle latency is maintained. In some cases, retiming does involve adding registers.

Pipelining is a design time decision where the architecture incorporates registers.

Both are done to alleviate timing violations, but occur at different time in the flow.

# Transistor Sizing

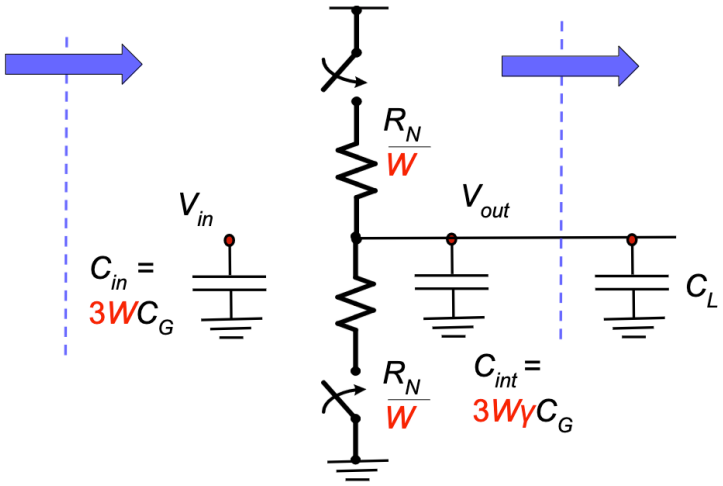
- Sizing is modifying the transistor gate width
  - Increasing the gate width by a scale factor $W$
    - $R \propto 1/W$, $C \propto W$
- PMOS (classic) have about twice the resistance of NMOS because of mobility of of holes
  - For symmetry for size PMOS so resistance matches NMOS
  - The resistance of PMOS is similar in modern process
- Parasitic capacitances on gate, source, and drain
  - $C_D = \gamma C_G$




https://static.designandreuse.com/news_img17/20170201_1.jpg

# Inverter Delay with Load

**Delay proportional with fanout!**




$$t_p = 0.69(R_N/W)(C_{int} + C_L)$$

$$= 0.69(R_N/W)(3W\gamma C_G + C_L)$$

*factor out* $3W\gamma C_G$

*replace* $C_{in} = 3WC_G$

$$= 0.69(3\gamma R_N C_G)(1 + \frac{C_L}{\gamma C_{in}})$$

$$= t_{p0}(1 + \frac{C_L}{\gamma C_{in}}) = t_{p0}(1 + f/\gamma)$$

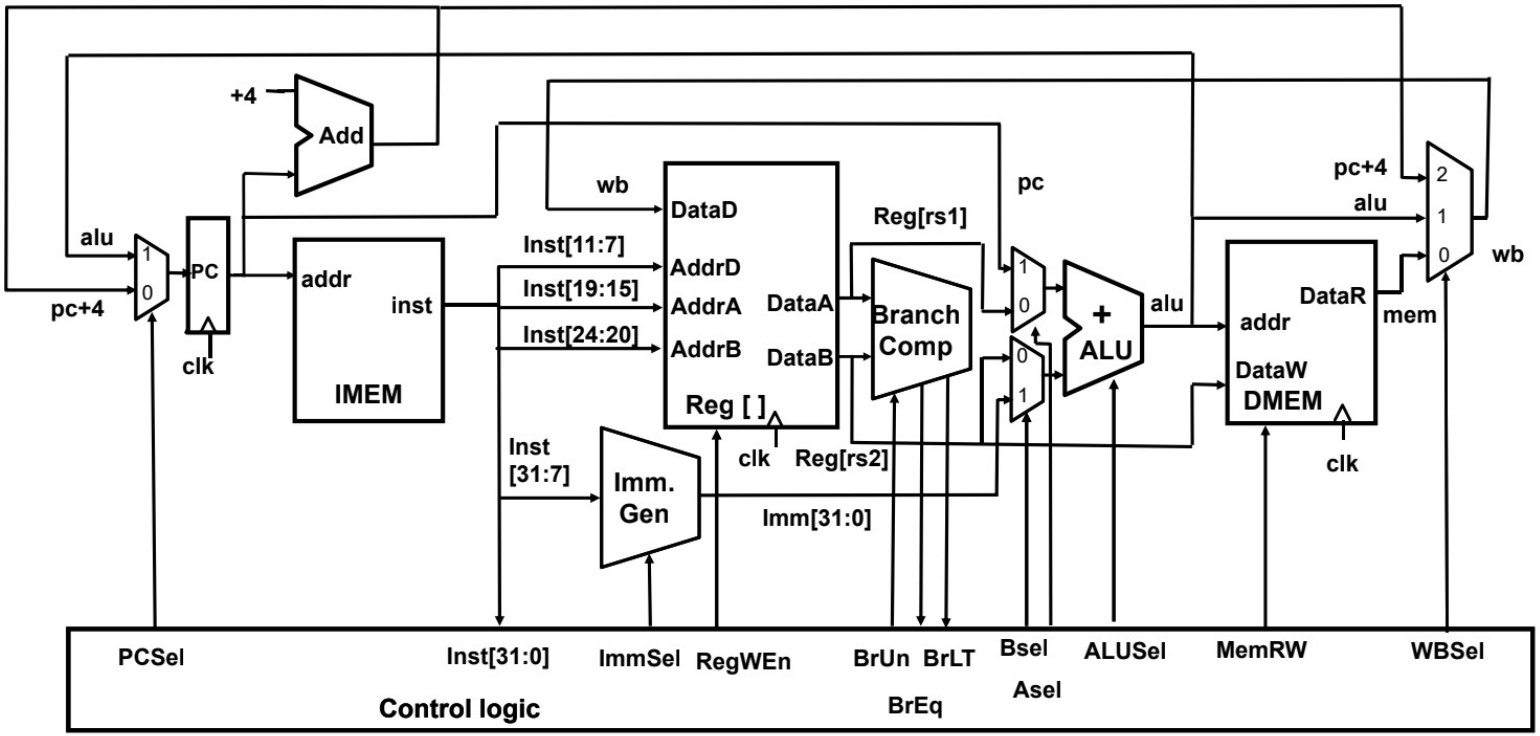
***f*** = **electrical fanout** = ratio of load capacitance ($C_L$) to and input capacitance ($C_{in}$)

# Delay Optimization

- Delay optimization at this level is simplified and based off an inverter
  - Inverters are common in CMOS processes (ex. buffers)
  - Understanding can be extracted to more complex gates
- A symmetric inverter in a planar process :
  - Not driving a load: $t_{1/2} = \ln(2)\, R(3\gamma C_G)$
  - Driving a load: $t_{1/2} = \ln(2)\, R(3\gamma C_G + C_L) = t_{p0}(1 + \frac{C_L}{\gamma C_{in}})$
    - Fanout $f = \frac{C_L}{C_{in}}$, therefore $t_{1/2} = t_{p0}(1 + \frac{f}{\gamma})$
- Fanout of 4 (FO4)
  - A rule of thumb for creating chain of gates
  - Circuit is optimal as far as delay is fanout is ~4
  - Often optimal fanout is less than 4 in reality

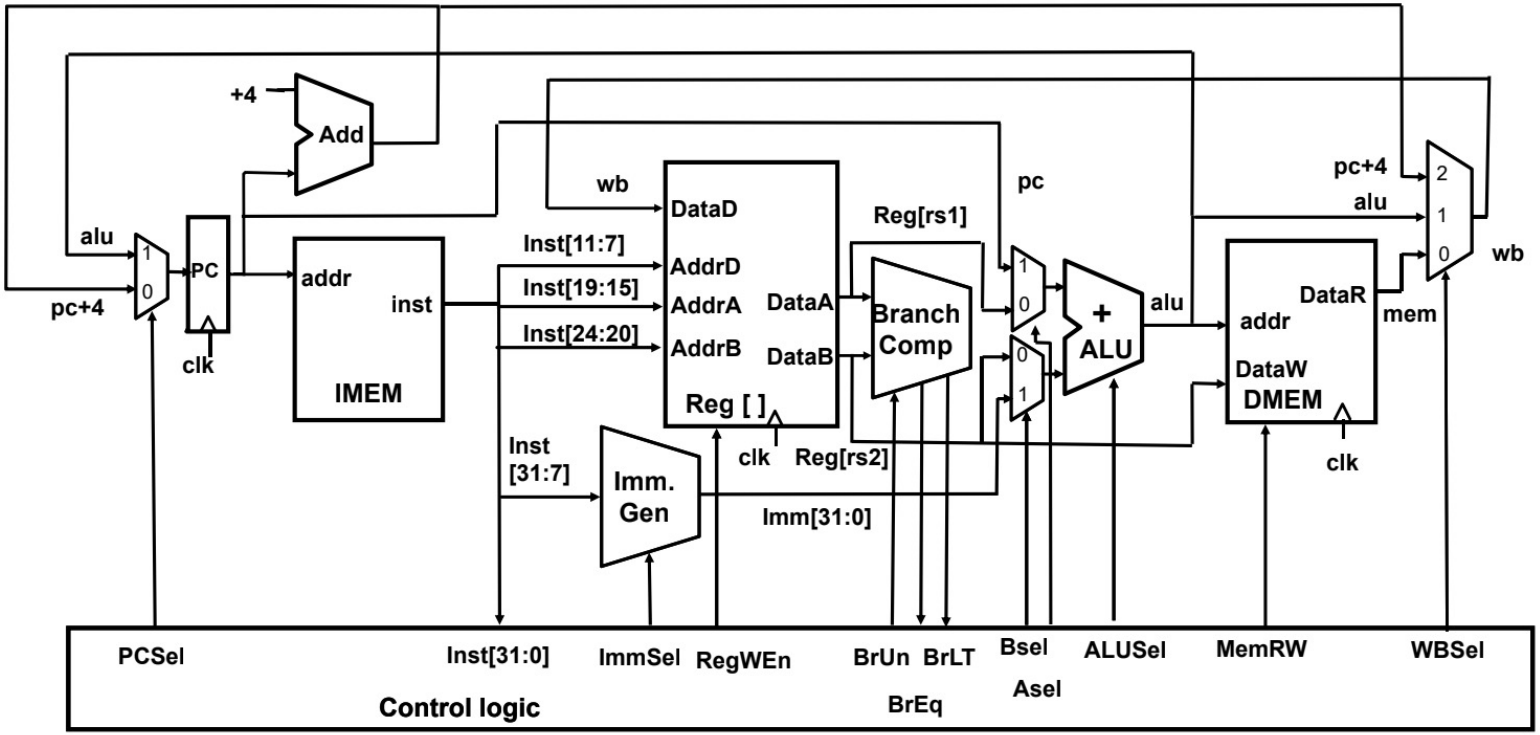
# Single Cycle RISC-V

- One instruction fetched per cycle, one cycle per instruction execution



# Problem 1

- Which instruction type dictates the clock frequency? Draw the path on the diagram below.



# Problem 1

- Which instruction type dictates the clock frequency? `lw`
  Draw the path on the diagram below.