EECS 151/251A Discussion 7

Friday 1st March, 2024

Problem 1. Retiming

Consider the circuit below. What is the maximum clock frequency? Retime the circuit to minimize the critical path delay. What is the maximum clock frequency for the retimed circuit? Also show the diagram of the retimed circuit. The FFs have $t_{setup} = 10\text{ps}$, $t_{clk-q} = 10\text{ps}$, and $t_{hold} = 5\text{ps}$.