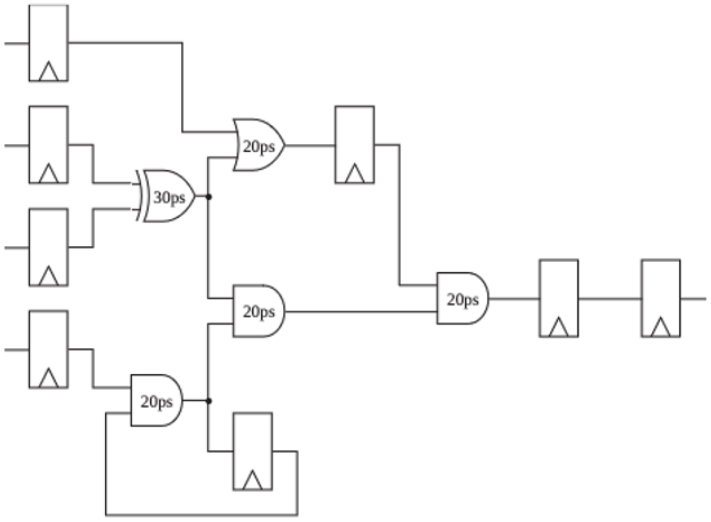
EECS 151/251A Discussion 7

Friday 1st March, 2024

Problem 1. Retiming

Consider the circuit below. What is the maximum clock frequency? Retime the circuit to minimize the critical path delay. What is the maximum clock frequency for the retimed circuit? Also show the diagram of the retimed circuit. The FFs have $t_{setup} = 10\text{ps}$, $t_{clk-q} = 10\text{ps}$, and $t_{hold} = 5\text{ps}$.



Solution:

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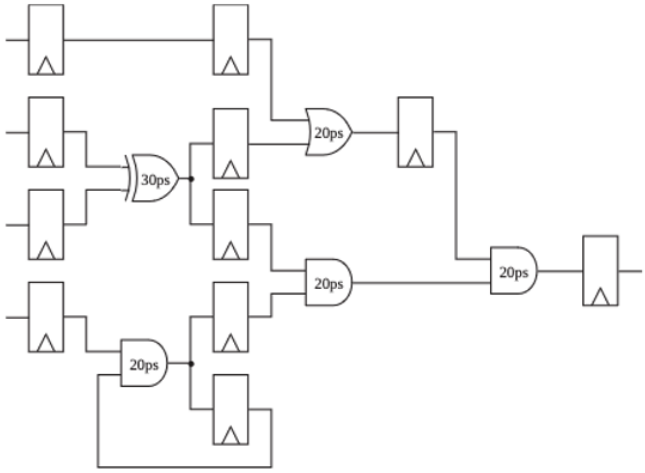
Original maximum clock frequency: $\frac{1}{10+10+30+20+20\text{ps}} \approx 11.1\text{GHz}$.
(The hold time constraint does not matter because clock to q delay is larger.)
Retimed maximum clock frequency: $\frac{1}{10+10+20+20\text{ps}} \approx 16.6\text{GHz}$.
Diagram:



Note: The following diagram is wrong because it merges two FFs at the fanout of XOR gate even though we are not given initial values of FFs.