EECS 151/251A Final Exam Information

Spring 2024

The exam will take place Tuesday May 7, 11:30AM–2:30PM in Physics Building 3 and Evans 60. Check ed posts for which room you have been assigned. All students are allowed *two* 2-sided 8.5×11 inch sheet of notes. No calculators, phones, or other electronic devices will be allowed. Slide-rules will be permitted.

The final exam will be comprehensive and test all topics covered this semester. However, emphasis will be placed on topics covered after the midterm exam—those listed below.

Topics:

1. Origin and consequences of delays and constraints associated with registers (setup, hold, "clock to q")
2. Maximum clock frequency calculation from circuit parameters
3. Origin of gate-delay and calculation, effects of transistor sizing
4. Delay property of wires and rebuffering
5. Circuit register rebalancing
6. Logic delay combined with wires
7. Driving large capacitive loads
8. How to Design a RISC-V Single-Cycle Processor from the ISA
9. Processor Pipelining Hazards and Mechanisms
10. Sources of Power and Energy consumption in Digital ICs
11. Principles of Low-power Design Techniques
12. How to Improve Energy Efficiency through Parallelism and Pipelining
13. Memory Block Internal Architecture
14. SRAM Cell and Read/Write Operation
15. Memory Block Periphery Circuits

16. Memory Decoder Design
17. DRAM Cell and Read/Write Operation
18. Dual-port Memory Architecture
19. Cascading Memory blocks for More Width, Depth, and Ports
20. FIFO Implementation
21. Serialization versus Parallelization in Iterative Computations
22. Principles of Pipelining and Restrictions of Loops
23. List-processor Design and Optimizations
24. Carry Select Adder Design
25. Carry Lookahead and Parallel Prefix Adders
26. Bit-Serial Addition
27. Array Multiplier Design
28. Carry Save Addition
29. Signed Multiplication
30. CSD Multiplier Design
31. Log and Barrel Shifters Design and Analysis
32. Cross-bar Switch Design and Operation
33. Effect of Clock Uncertainties on Maximum Clock Frequency and Race Margin
34. Source of Clock Uncertainties
35. Principle of Good Clock Distribution