EECS 151/251A Homework 6

Due Monday, March 4rd, 2024

Introduction

This homework is meant to exercise your understanding of CMOS circuits. For your submission, please make sure any circuits are drawn with a schematic maker or hand drawn cleanly (include drawings on tablet devices). Also, for clarity, please signify connections between two wires with solder joints (dots where wires are connected, are highly recommended).

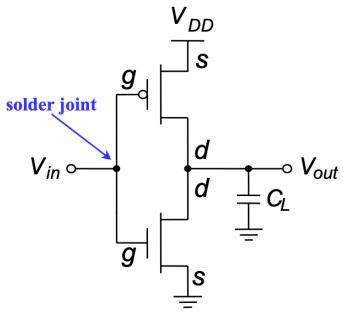
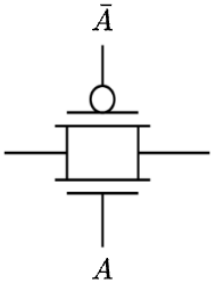


Figure 1: CMOS inverter schematic with solder joints

Problem 1: Static CMOS Circuit

A transmission gate is a simple structure composed of two transistors which operates like a switch. Answer the follow questions to understand their functionality and use.

1. What is the benefit of using a transmission gate compared to a single transistor?
2. Explain in words how a transmission gate functions when a single input and its complement are presented to the NMOS and PMOS gates respectively as shown below.



3. How can a transmission gate be used to tri-state the output of a gate? For example, as with a tri-state buffer?

Solution:

1. For a quick understanding view this link: https://www.allaboutcircuits.com/technical-articles/the-cmos-transmission-gate/.

   Having a transmission gate reduces the overal resistance of the path. Also, in CMOS it easier to fabricate a transmission fate.

2. If A is logical high, then both MOSFETs turn on and allow current to pass. The exact opposite happens if A is logical low. If A is logical low, then both MOSFETs are off and prevent current flow. As consequence, the output is not driven to a given voltage (logic) level and is left floating (this is high-Z or high-impedance).

   Points will be deducted if both cases of logical level are not discussed, and reference to floating the output is not discussed in the provided answer.

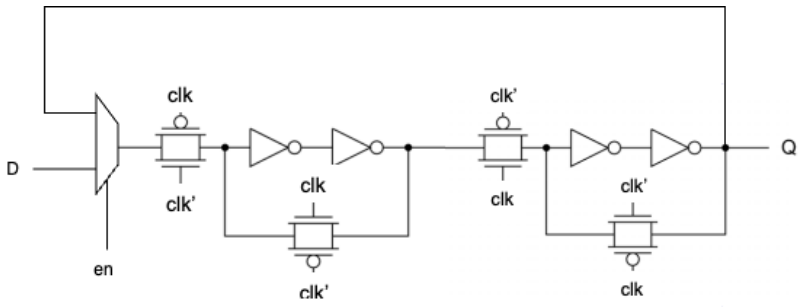
3. Place the transmission gate at the output of the gate and tie an enable signal as shown in the image above. If the enable is logic high, then the gate output is driven to the output of the transmission gate. If the enable is logic low, then the transmission gate output is floating and the logic gate is tri-stated.

Problem 2: Flip-Flop with Clock Enable

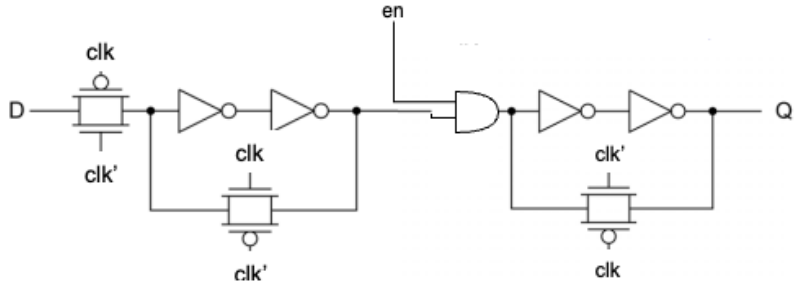
An implementation of a positive-edge triggered flip-flop using transmission gates was shown in lecture. Unlike many flip-flops used in real-world circuits, it does not have a clock enable. Modify the circuit from lecture to implement a flip-flop with a clock enable (*Hint: There are two ways to do this. Provide one of the two ways*).

Solution:

The first and possibly easiest way is to use a mux.



The second way is to use an AND gate.



Problem 3: Circuit-to-Boolean-to-Verilog

Below we display a schematic for a common function in digital circuits implemented in CMOS.

Complete the following for this circuit:

1. Write its Boolean expression
2. Explain in words what this circuit does
3. Provide a continuous assignment statement representing this circuit.

Solution:

1. The expression for the pull down network is $\bar{A}(\bar{B}+\bar{C})+A\bar{B}\bar{C}$. The expression for the pull up network is its complement.

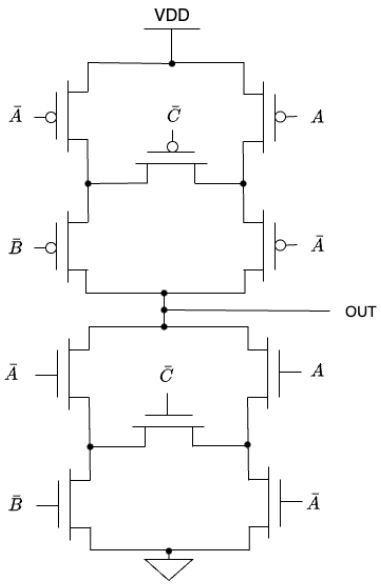


Figure 2: Schematic of CMOS

2. If two of the three inputs are logical low, then the output is low. Therefore, if two or more of the inputs are logic high, then the ouptut is high. This is the majority function.

3. `assign majority = ~A&(~B+~C) + A&~B&~C;`

Problem 4: Layout Practice

Below we present a layout for a five input CMOS circuit. Complete the following:

1. A gate-level schematic of the circuit
2. The Boolean expression for the pull-down network.

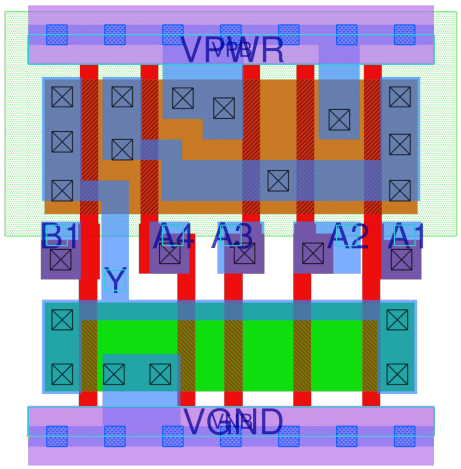
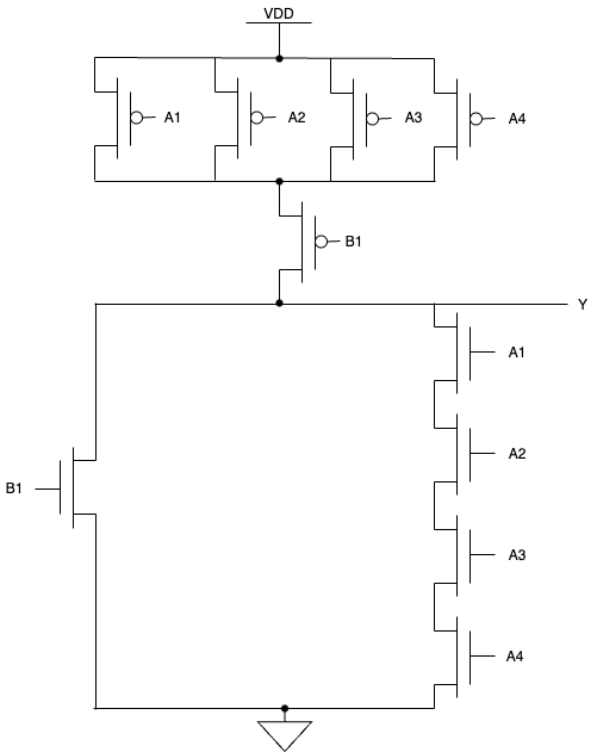


Figure 3: Layout of a unnamed circuit

Solution:

1.

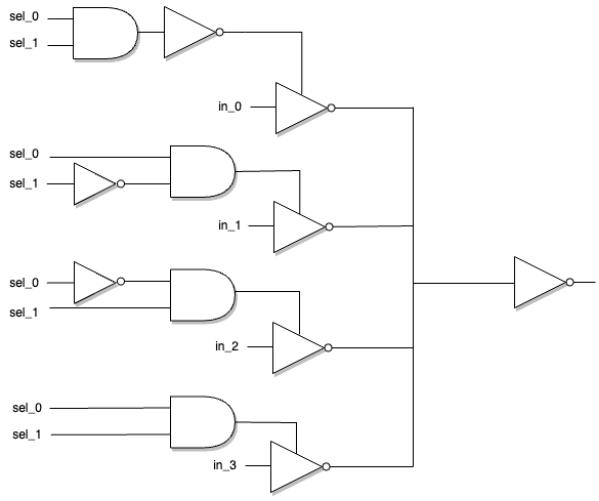


2. $B1 + A1\&A2\&A3\&A4$

Problem 5: 4-to-1 Multiplexor with Transmission Gates

Draw gate-level circuit diagram for a tri-state based 4-to-1 multiplexor using no more than four tri-state inverters, along with simple logic-gates, if needed.

Solution:

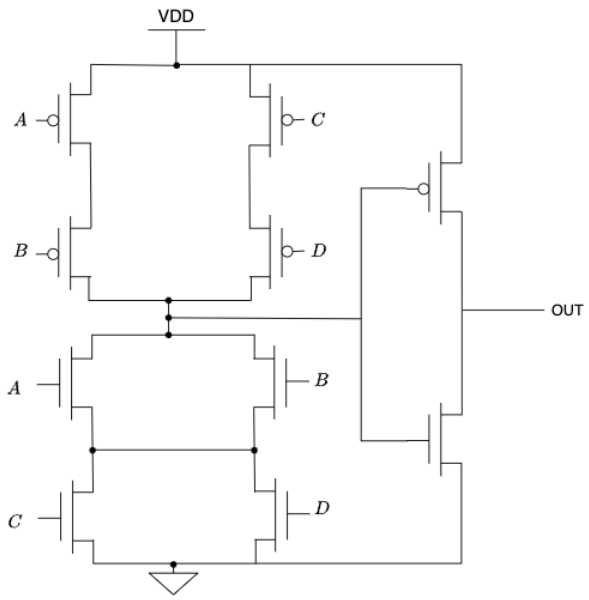


Problem 6: Static Circuit

Draw a transistor-level schematic for the Boolean expression $(A+B)(C+D)$ in the "static CMOS style" (as presented in lecture) using the minimal number of transistors. You are not provided with complemented inputs (*Hint: You need to create the complements*).

Solution:

Note this is the best solution. The hint was there to make you realize that every gate input would need to inverted. When this is the case the output can just be inverted which greatly reduces the number of inverters (push bubbles).



Problem 7: Negative-Edge Trigged Flip-Flop

Draw the gate-level schematic for a negative-edge triggered flip-flop built using the "Tri-State-Inverter" style latch presented in lecture.

Solution: