

EECS 151/251A LTspice Tutorial

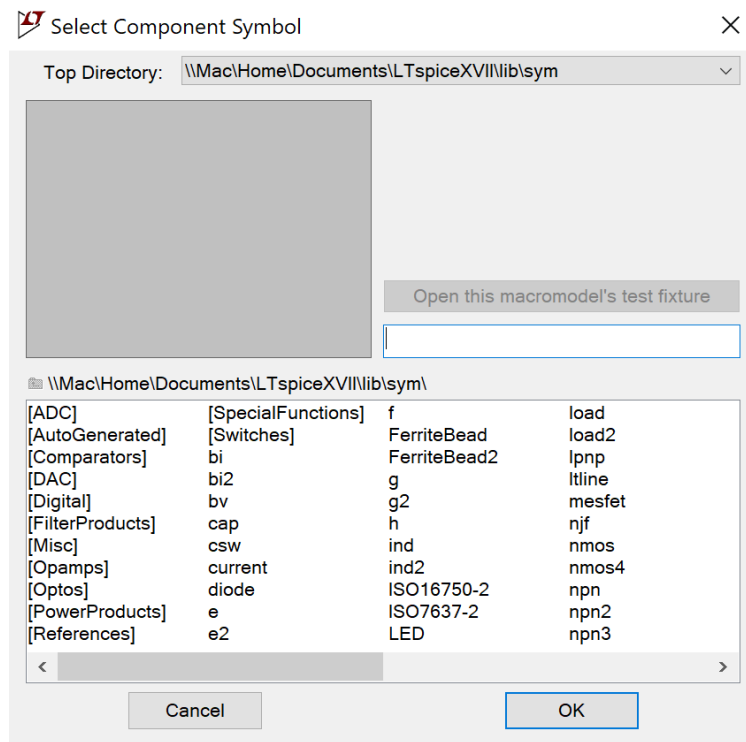
1 Installing LTspice

Download and install LTspice here: <https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html>

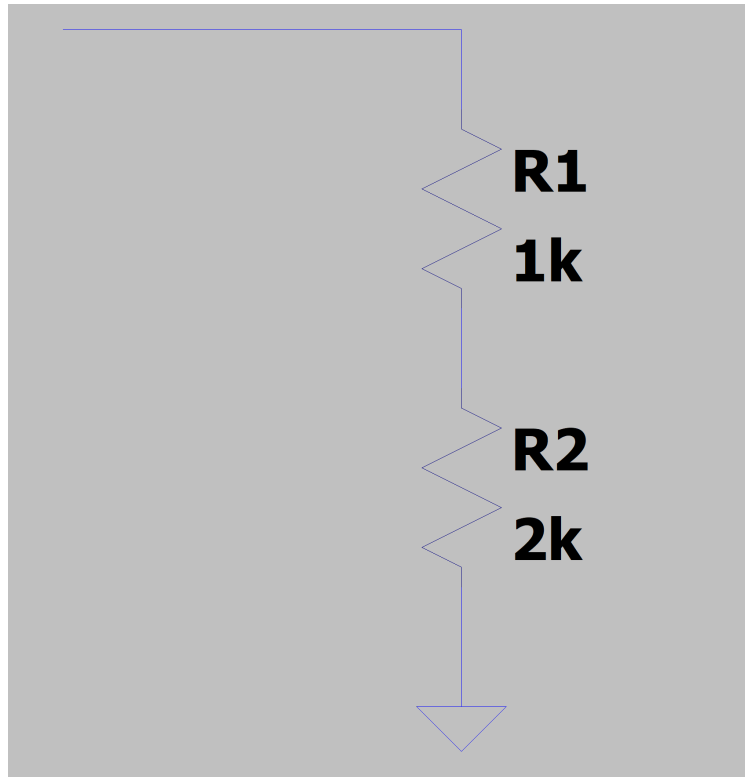
2 Creating a Schematic

Start a new blank schematic from **Files > New > New Schematic** or **Ctrl-N/Cmd-N**.

For the tutorial let's build a simple resistive voltage divider. You can add a component by right-clicking and going to **Draft > Component**. LTspice will bring up a menu that looks like the following:

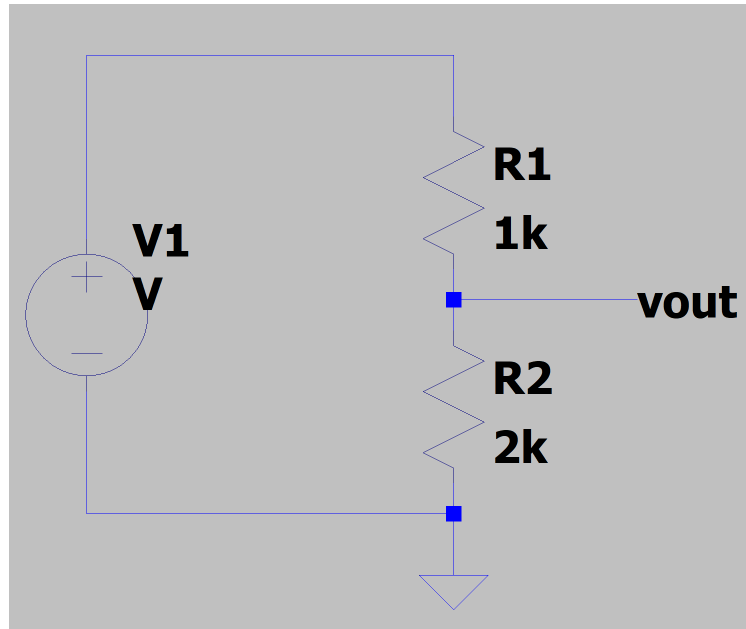


You can use the search bar to search for resistors. Now place two resistors on your schematic and right-click on the resistors to assign values to them. For the tutorial let's use 1 k Ω and 2 k Ω resistors for R1 and R2. Right-click and go to **Draft > Draw Wire** to connect the two resistors. Press **G** to place ground on R2. It may be helpful to map the Component and Draw Wire to hot-keys for quicker access or use the default keyboard shortcuts. Your schematic should look like the following:



If you need to move, drag, duplicate, or delete wires or components, you can select these commands by right-clicking and going to **Edit**. Again, you can map these commands or use the default keyboard shortcuts.

Now, add a voltage source by going to the component menu and search for "voltage". Right-click the voltage source and assign it a default value of 0V. Place it in your schematic and connect it to R1 and ground. Place a wire between R1 and R2 and label the net as **vout** by going to **Draft > Label Net** or **Draft > Net Name** (for Mac). Your schematic should look like the following:



3 Running a DC Analysis

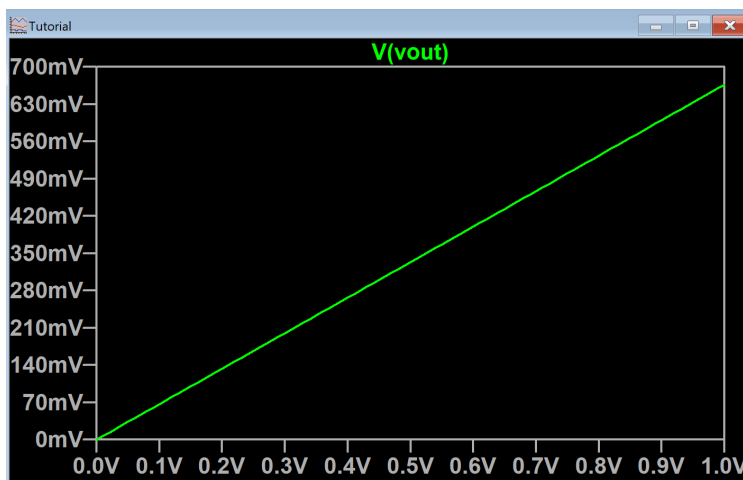
To run a DC Analysis, you can enter in the spice directive manually by pressing **S** or right-clicking and going to **Draft > SPICE directive**. The command for a DC Analysis is formatted as follows.

```
.dc <srcnam> <Vstart> <Vstop> <Vincr> [<srcnam2> <Vstart2> <Vstop2> <Vincr2>]
```

For our case, let's sweep V1 from 0 to 1 V with 0.01 V increments. So the command will be

```
.dc V1 0 1 0.01
```

Place the spice directive somewhere on your schematic. To run the simulation, right-click and select **Run**. An empty graph will pop up. You can see the voltage for vout by clicking on its net or right-click and select **Add Trace** and select **V(vout)**. You should see something like the following:



This looks right, since v_{out} is $2/3$ of the applied voltage, which is the correct resistor divider ratio from the given resistor values.

4 Importing the 16nm Transistor Model

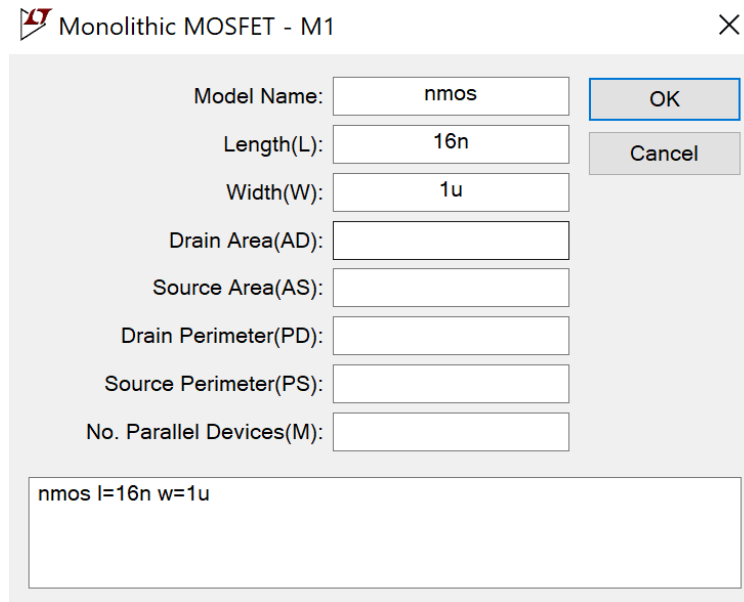
Create a new schematic. Download the 16nm process technology provided on http://ptm.asu.edu/modelcard/LP/16nm_LP.pm. Your browser may save it as `16nm_LP.pm.txt`, which is fine, just make sure to include the full file name in the command. To use the model, create a spice directive with the following command:

```
.include <path to 16nm_LP.pm>
```

If you placed the model in the same directory as your schematic, your command will look like

```
.include ./16nm_LP.pm
```

To place an NMOS or PMOS transistor onto your schematic, bring up the component menu and search for `nmos4` and `pmos4`. After placing it, right click on the component and you will get a menu that looks like the following. For NMOS devices, put in `nmos`, and for PMOS devices put in `pmos`. This is because the 16nm model file defines the model as such. You will have to assign a Length and Width for these devices. We will provide you the values to use in homework problems. For example, to create an NMOS device with a Length of 16 nm and Width of 1 μm , your menu should look like the following:



Monolithic MOSFET - M1

Model Name:

Length(L):

Width(W):

Drain Area(AD):

Source Area(AS):

Drain Perimeter(PD):

Source Perimeter(PS):

No. Parallel Devices(M):

nmos l=16n w=1u

Note: Because MOSFETs are 4-terminal devices, you will need to tie the body of NMOS's to GND and the body of PMOS's to VDD.

5 Acknowledgements

16nm Process Technology Model courtesy of the PTM group at ASU. <http://ptm.asu.edu/>